CLMPTO
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1. An opto-electronic device, comprising:

a substrate comprising a first III-V semiconductor layer;

an electrically insulating layer that extends on the first III-V semiconductor layer and comprises an array of non-photolithographically defined nanopores therein;

an array of vertical quantum-dot superlattices in the array of nanopores; and

a second III-V semiconductor layer on said array of vertical quantum-dot superlattices.

2. The device of Claim 1, wherein the nanopores in the array have an average diameter in a range between about 8nm and about 50 nm.

3. The device of Claim 1, wherein the first III-V semiconductor layer is an N-type semiconductor layer; and wherein the second III-V semiconductor layer is a P-type semiconductor layer.

4. The device of Claim 1, wherein the first III-V semiconductor layer is an N-type $Al_xGa_{1-x}As$ layer; and wherein the second III-V semiconductor layer is a P-type $Al_xGa_{1-x}As$ layer.

5. The device of Claim 1, wherein the first III-V semiconductor layer comprises an N-type GaAs layer and an N-type $Al_xGa_{1-x}As$ layer on the N-type GaAs layer.

6. The device of Claim 5, wherein said electrically insulating layer comprises an anodized aluminum oxide layer having the array of non-photolithographically defined nanopores therein.

7. The device of Claim 6, wherein each of a plurality of vertical quantum-dot superlattices in the array of nanopores comprises an alternating arrangement of InGaAs and GaAs dots therein.

8. The device of Claim 7, wherein said second III-V semiconductor layer comprises a P-type $Al_xGa_{1-x}As$ layer that contacts said electrically insulating layer and a P-type GaAs layer that extends on the P-type $Al_xGa_{1-x}As$ layer.

9. The device of Claim 5, wherein said electrically insulating layer comprises a silicon dioxide layer having the array of non-photolithographically defined nanopores therein.

10. The device of Claim 9, wherein each of a plurality of vertical quantum-dot superlattices in the array of nanopores comprises an alternating arrangement of InGaAs and GaAs dots therein.

11. The device of Claim 10, wherein said second III-V semiconductor layer comprises a P-type $Al_xGa_{1-x}As$ layer that contacts said electrically insulating layer and a P-type GaAs layer that extends on the P-type $Al_xGa_{1-x}As$ layer.

CLAIMS 12-16. (CANCELLED)